

JUN 20 2008



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DATE: June 20, 2008

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COMMENTS:

Attached please find the Agenda for the Examiner Interview on June 24, 2008 at 12:00 p.m. MST regarding the below patent application:

Application No. 10/774,990
Filing Date: 02/09/2004
Inventor: Matthew J. Amatangelo
Attorney Docket: 188082/US
Confirmation No. 9588
Art Unit: 2128
Office Action Date: 02/28/08

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REFERENCE #481214-24 (188082/US)

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Agenda for Examiner Interview on 6-24-08, 12 pm MST re: application 10/774,990

1. 112 Rejections

a. Indefiniteness rejections

1. Particular terms

- i. evaluate node – see Zhao reference, section I, 2nd paragraph, also see application para. 34
- ii. dynamic circuit – common in the art (see textbook figures)
- iii. labeling – see application para. 42 (labeling = inserting a keyword)
- iv. near dynamic circuit – see application para. 9 (near domino is a species of the genus near-dynamic, just as domino is a species of the genus dynamic)
- v. dynamic signal – common in the art

b. Incomplete rejection (omitting essential steps)

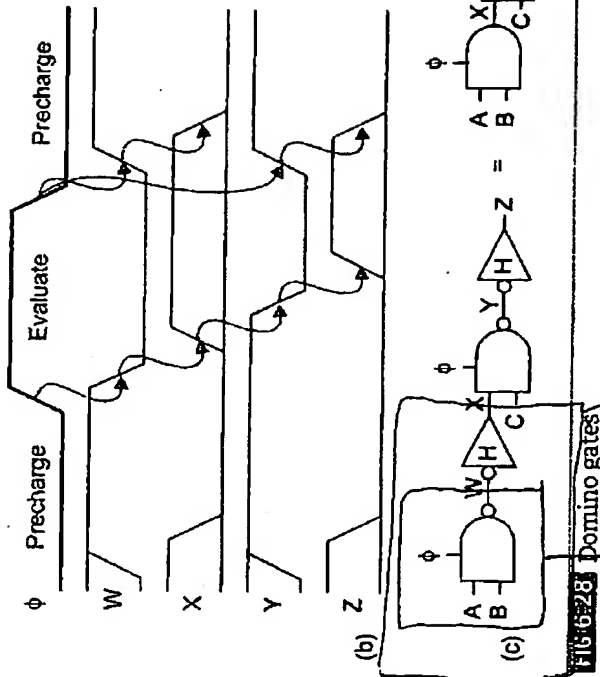
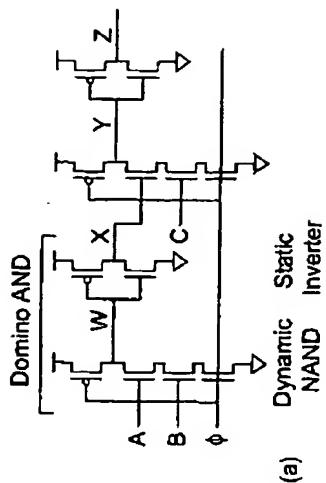
1. ??

2. 101 Rejections

- a. proposed change 'propagating' to 'modeling' in claim 1

3. 102 Rejections

- a. Norton labels the nodes as either clock, data, dynamic, latch, or gated. The present invention labels them as "near dynamic"



true domino
true dynamic

From CMOS VLSI Design
A Circuits and Systems Perspective
(3rd Edition)
Neil Weste and David Harris
Addison Wesley
ISBN: 0-321-14901-7

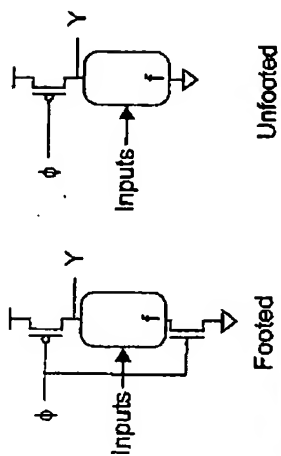


FIG 6-24 Generalized footed and unfooted dynamic gates

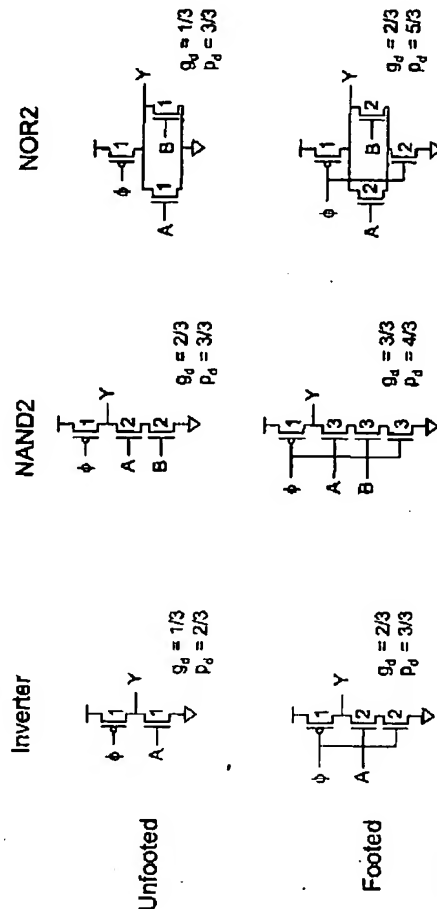


FIG 6-25 Catalog of dynamic gates

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